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| Speaker and Author: | Jeanne Trinko Mechler - GLOBALFOUNDRIES, Essex Junction, VT |
| Title: DFT design challenges for next generation 7nm FinFET applications |  |  |

Jeanne Trinko Mechler, is a fellow in the GLOBALFOUNDRIES ASIC worldwide design organization. After 30 years of chip design experience working for the IBM Systems & Technology Group in Essex Junction, VT, she joined GLOBALFOUNDRIES in 2015. She holds patents and has published papers in the areas of design for test, reliability, failure analysis, and SOC design. She has completed more than 35 custom logic designs and is currently working on 7nm and 14nm FinFET chip design. She specializes in networking chips and is an author of the engineering textbook High Speed SerDes Devices and Applications. She received the M.S. and B.S. in electrical engineering from the University of Vermont in 1989 and 1985 respectively, and the M.S. in engineering management from the National Technological University in 1992.

